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Nokia Care Academy

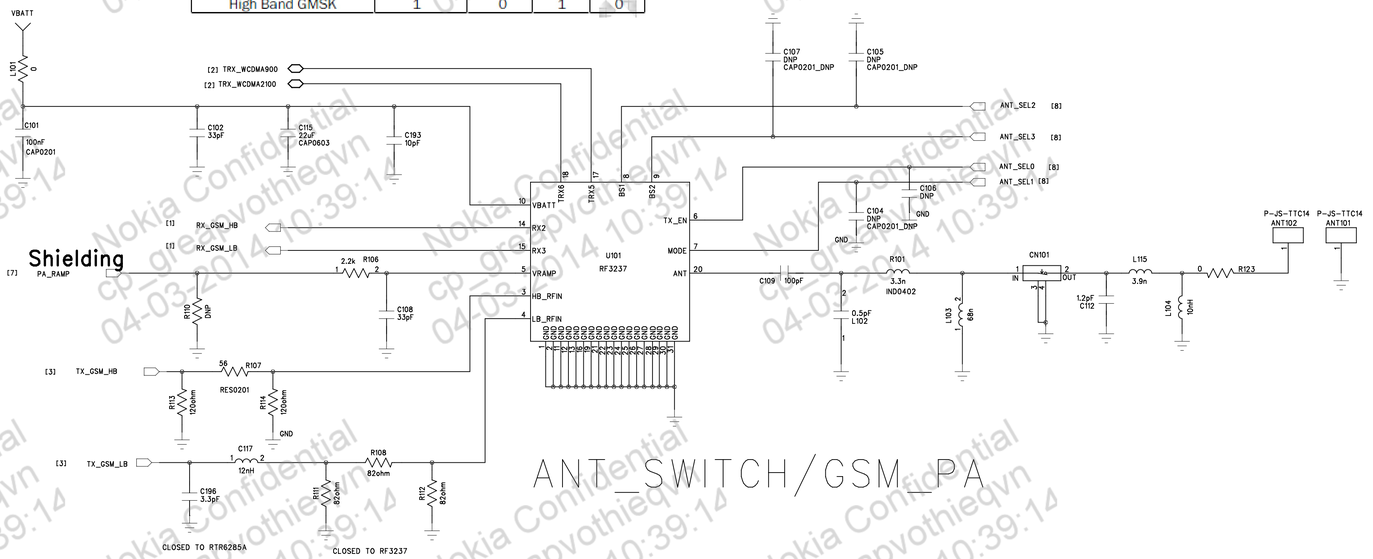
Nokia RM-980 Service Schematic and placement Manual

RM-980 V1.0

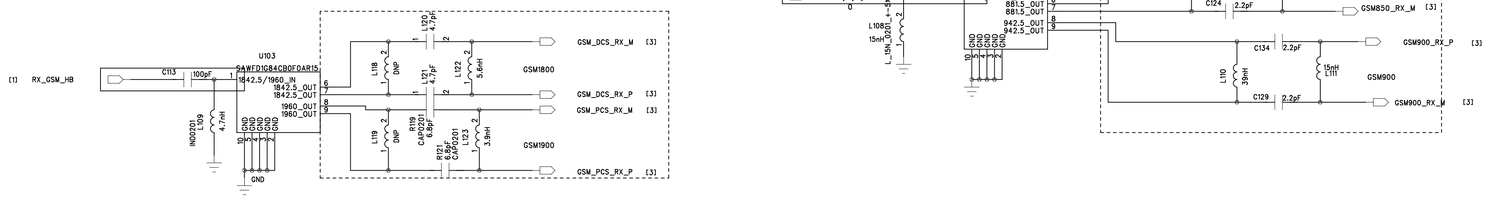
Schematics - Main board

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

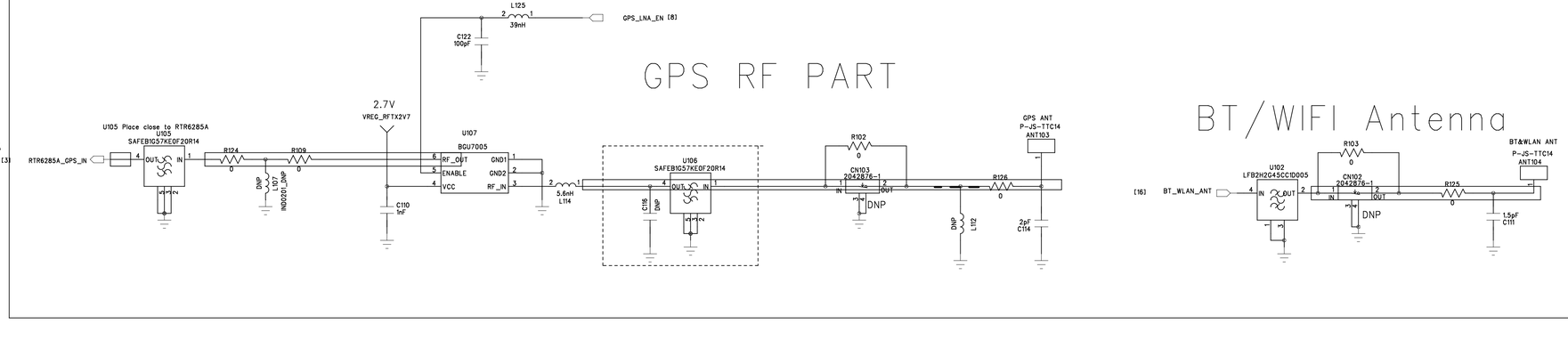
TX Module Mode	TX Enable	Mode	BS2	BS1
Off	0	0	0	0
WTRx2	0	0	0	1
WTRx3	0	0	1	0
WTRx5	0	1	0	1
WTRx6	0	1	0	0
Low Band GMSK	1	0	0	1
High Band GMSK	1	0	1	0



ANT_SWITCH/GSM_PA



GSM RX PART



GPS RF PART

BT/WIFI Antenna

COMPANY:	
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DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:
CODE:	SIZE:
DRAWING NO:	REV:
SCALE:	SHEET: 1 OF 16

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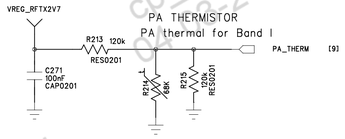
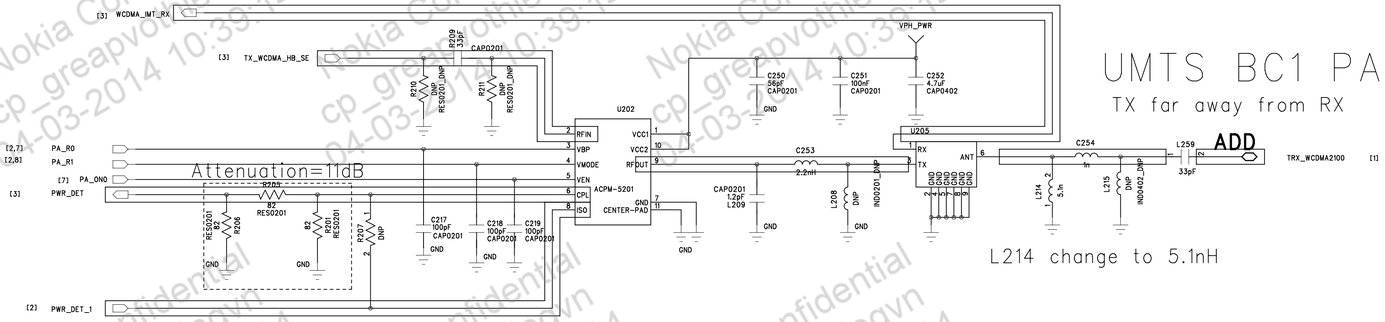
LTR	ECO NO:	APPROVED:	DATE:



BC1	Downlink	Uplink
IMT2100 Freq(MHz)	2110 ~ 2170	1920 ~ 1980

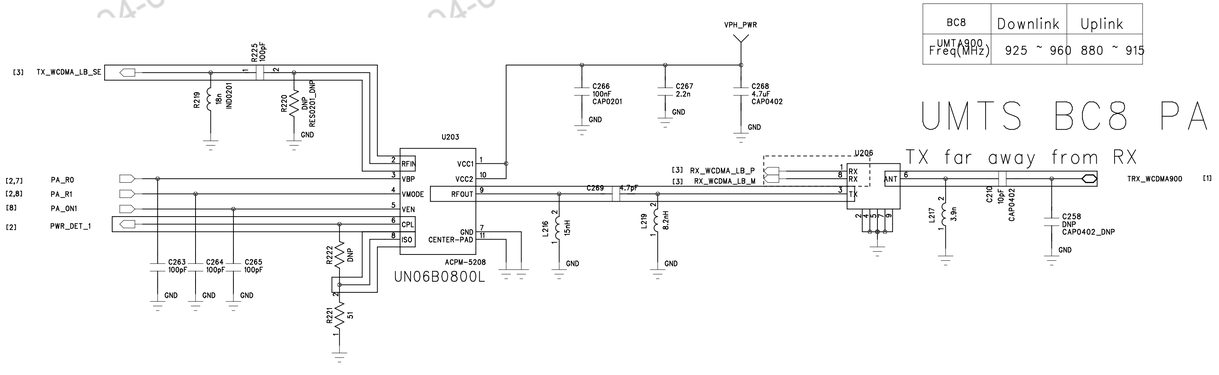


UMTS BC1 PA

TX far away from RX

L214 change to 5.1nH

BC8	Downlink	Uplink
UMTA900 Freq(MHz)	925 ~ 960	880 ~ 915



UMTS BC8 PA

TX far away from RX

DRAWN:	DATED:	COMPANY:		
CHECKED:	DATED:	TITLE: RF PA		
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO: REV:
RELEASED:	DATED:	SCALE:	SHEET: 2 OF 17	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Sheding

Sheding

Shielding

RF enable signal, used for enabling WCDMA TX and used as part of powerup sequence in GSM modes.

SSBI interface is used for WCDMA transmit power control. SSBI data digital CMOS input.
SSBI is used to control WCDMA transmit power. Hence, the TX_AGC_ADJ pin is no longer used.

U401-A
RTR6285A

Sheding

Shielding

TCXO

Shielding

RTR6285A POWER GRID

U401-B
RTR6285A

Shielding

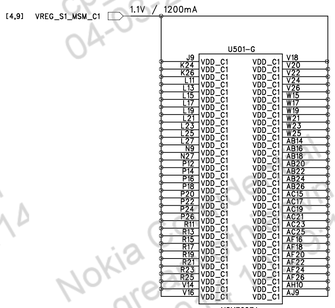
Shielding

UMTS BC1 SAW

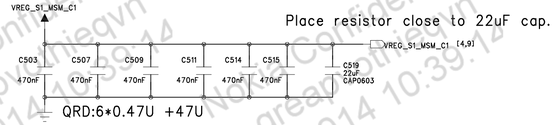
UMTS BC1 Rx Interstage

COMPANY:			
TITLE: RTR6285			
DRAWN:	DATED:	CODE:	SIZE: DRAWING NO: REV:
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: 4 OF 16

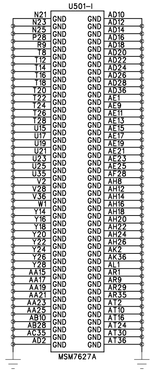
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

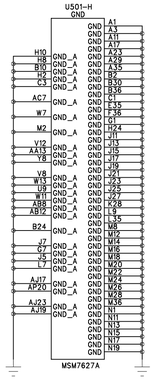


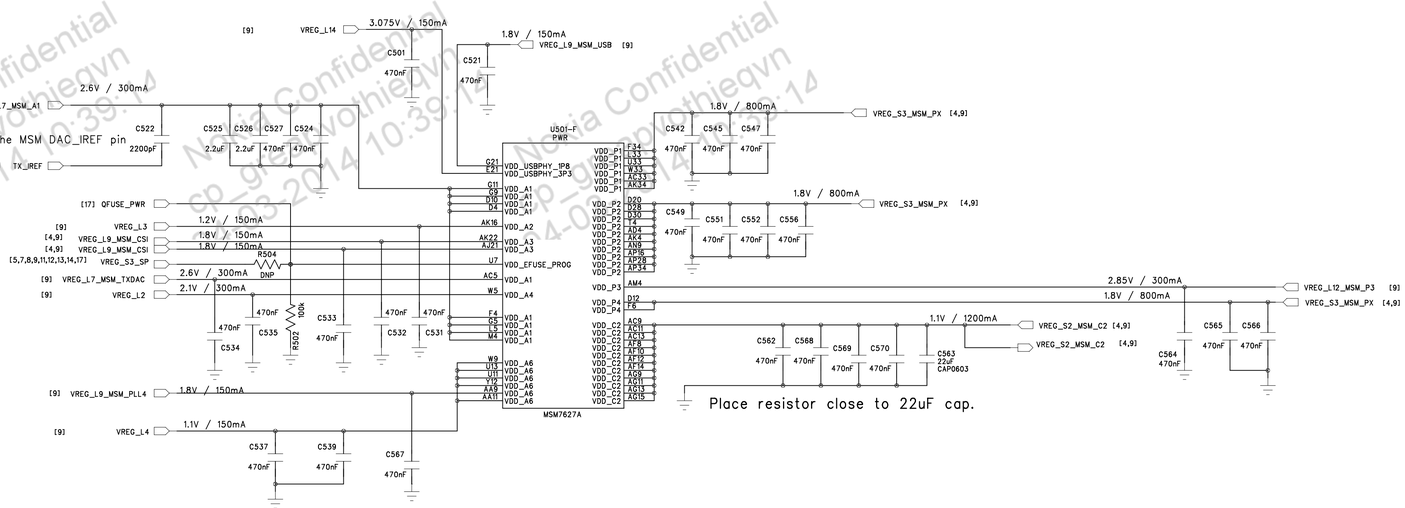
There are a total of 52 pins on MSM_C1.
These caps are to be shared by multiple power pins



Place resistor close to 22uF cap.







Place resistor close to 22uF cap.

VREG_L4_MSM_PLLX(X=0,1,2,3 and 5). Refer Device Spec (80-VM155-1)

Please connect pin U7 to 1.8V to program the efuse.(if need)

DRAWN:	DATED:	COMPANY:	
CHECKED:	DATED:	TITLE: MSM8225 PWR	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV:
RELEASED:	DATED:	SCALE:	SHEET: 5 OF 16

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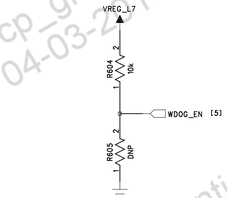
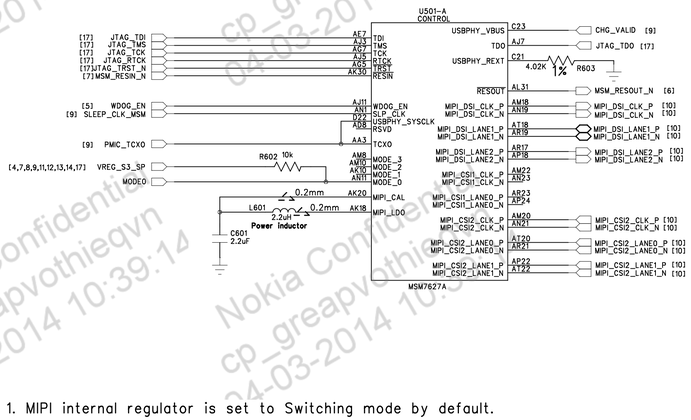
LTR	ECO NO:	APPROVED:	DATE:



Watch dog enable/disable select

WDOG_EN=0 DISABLE WDOG



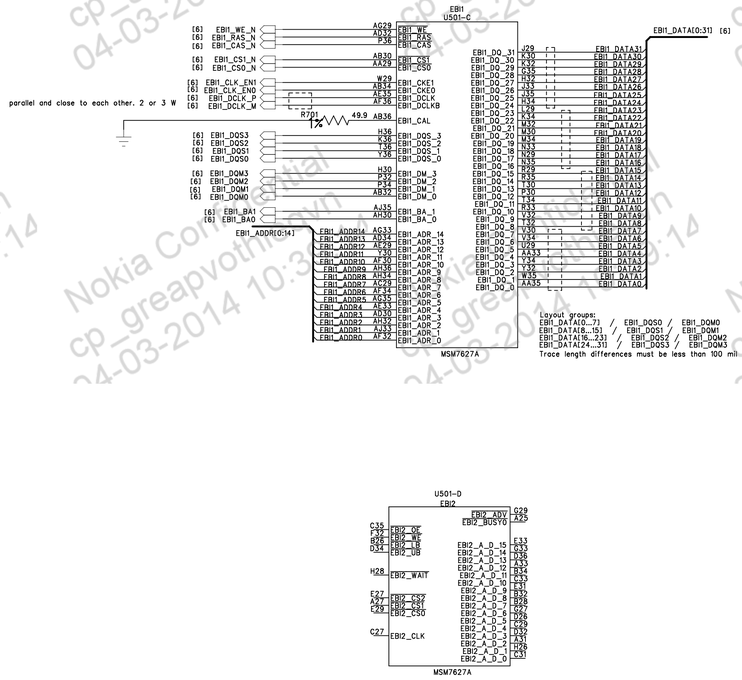
1. MIPI internal regulator is set to Switching mode by default.
   For LDO mode install 0 ohm instead of 2.2uH inductor.
2. MIPI signals should be routed as differential pair of 100 ohm impedance.

MODE[3:0]	MSM7X27A OPERATING MODE
0000	ARM9 on P_Jtag; ARM CORTEX A5 on A_Jtag
0001	ARM9 + ARM CORTEX A5 daisy chain on P_Jtag

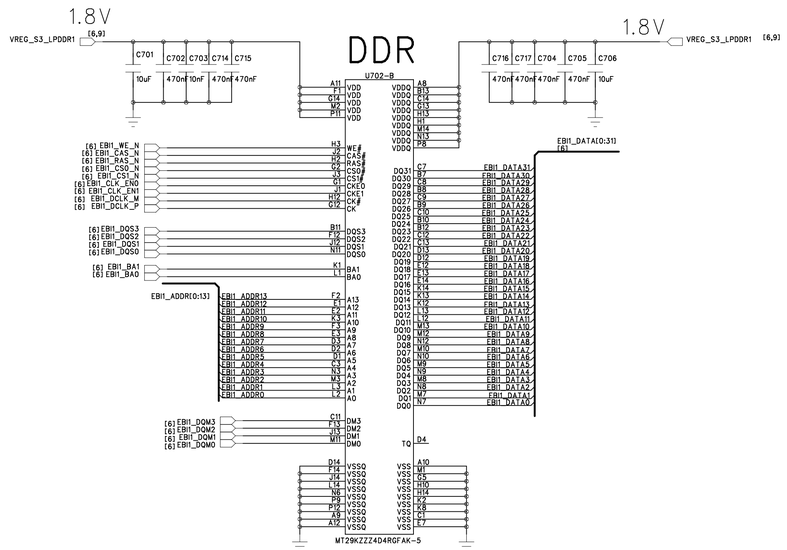
P_Jtag = Primary JTAG port, A_Jtag = Auxilliary JTAG port
MODE(3:0) pins have internal Pull Dowens.

DRAWN:	DATED:	COMPANY:			
CHECKED:	DATED:	TITLE: MSM8225 CTL			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
RELEASED:	DATED:	SCALE:		SHEET: 6 OF 16	

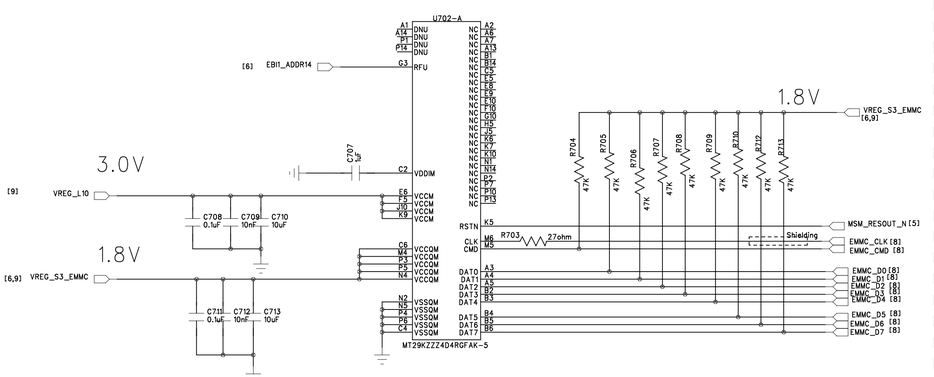
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DDR



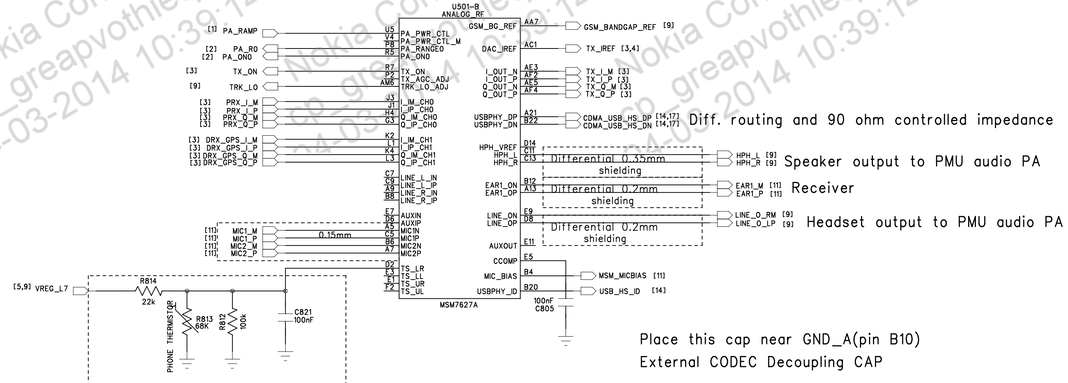
EMMC



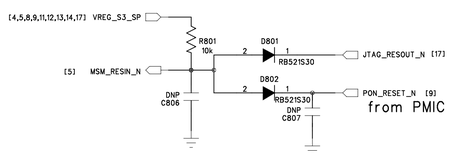
Hynix Memory MCP

DRAWN:	DATED:	COMPANY:			
CHECKED:	DATED:	TITLE: MSM8225 EBI MEMORY			
QUALITY CONTROL:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
RELEASED:	DATED:	SCALE:		SHEET: 7 OF 16	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



MSM THERMAL



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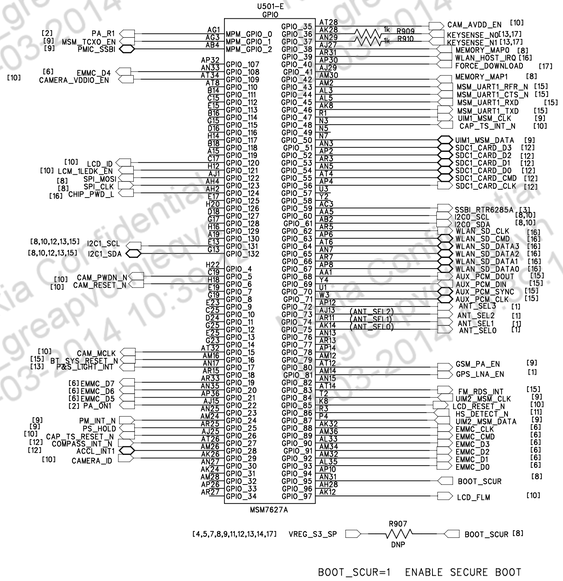
CHECKED:	DATED:				
QUALITY CONTROL:	DATED:				
RELEASED:	DATED:	SCALE:		SHEET: 8 OF 16	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



7 QRD DDR Auto Detection Implementation

7.1 Definition

QRD implements the lpddr1 auto detection by two GPIO pins.

NOTE: Be aware that this implementation needs hardware support. We use GPIO38 and GPIO42 as memory auto detection configuration. The detail definition is as in the Table 3:

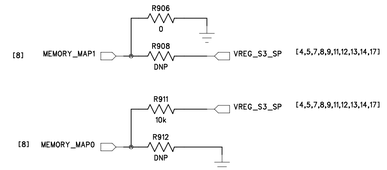
Vendor	Part Number	GPIO38	GPIO42
SANDISK	SD5D14A-4G	H	H
HYNIX	H9DP32A6AJACGR-KEM	H	L
SAMSUNG	Customer defined	L	H
MICRO	Customer defined	L	L

Table 3 Memory auto detection configuration

GPIO Values are as follows:

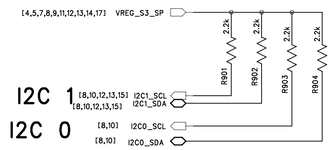
GPIO42	GPIO38	
1	1	= 0x3 SD5D14A-4G
1	0	= 0x2 SAMSUNG
0	1	= 0x1 H9DP32A6AJACGR-KEM
0	0	= 0x0 MICRON

Hynix Memory setting



Memory Auto detection
Hynix Memory MCP

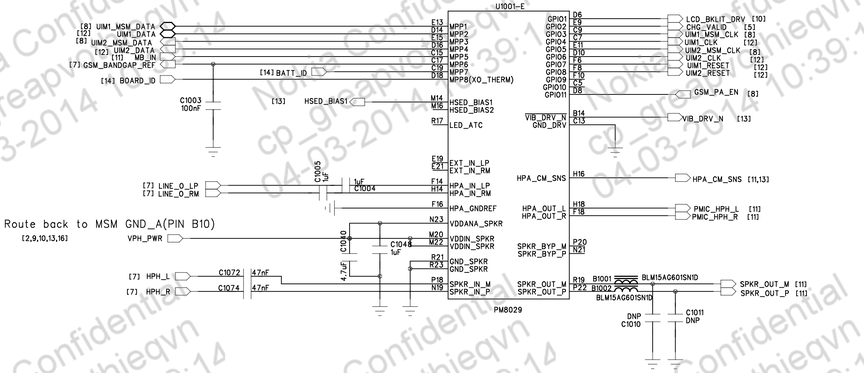
I2C bus pull high design

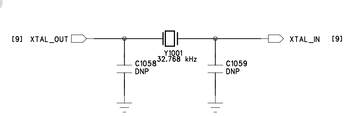


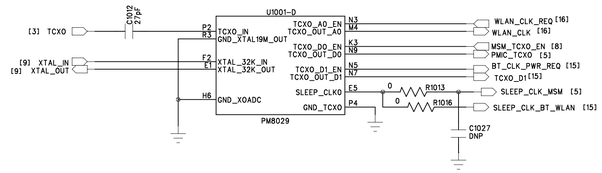
1. The PCM/I2S signals are muxed behind GPIO[68:71]. One of them can be used at a time while tri-stating the other in software.

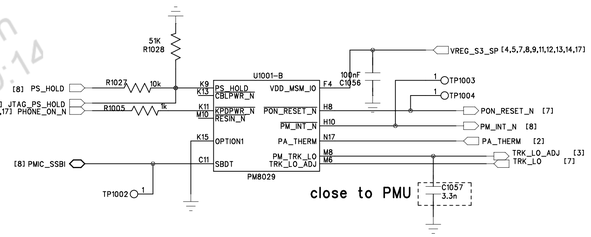
DRAWN:	DATED:	COMPANY:	
CHECKED:	DATED:	TITLE: MSM8225 GPIO	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO: / REV:	
RELEASED:	DATED:	SCALE:	SHEET: 9 OF 16

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

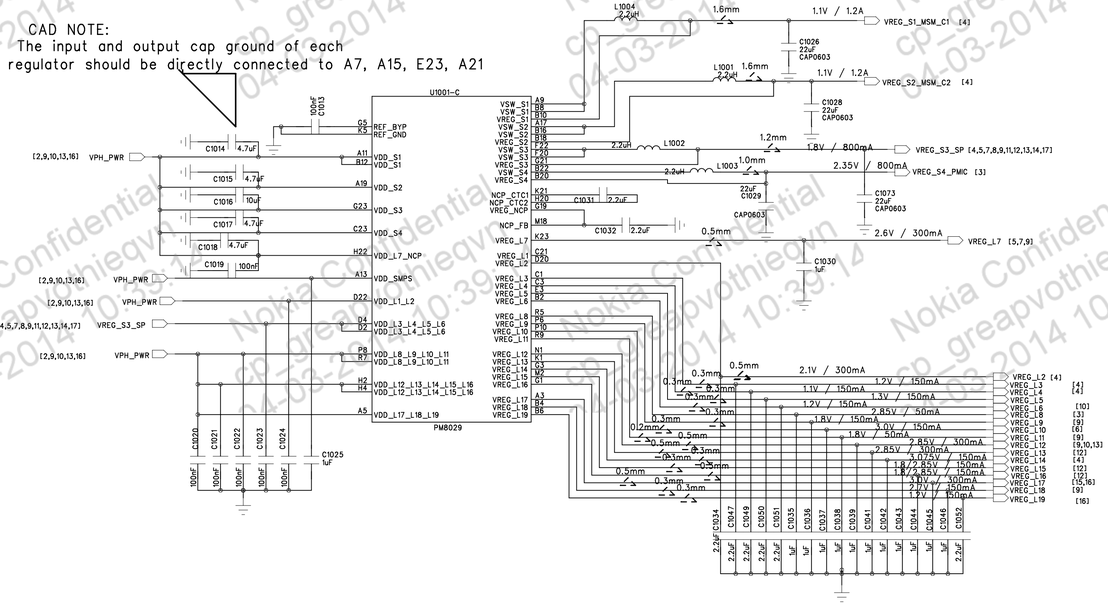


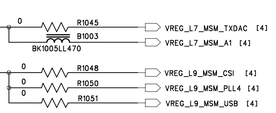


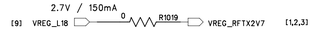


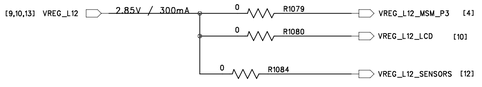


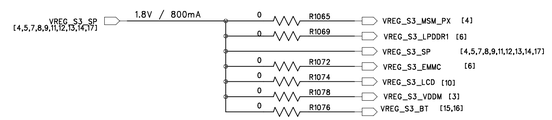
CAD NOTE:
The input and output cap ground of each regulator should be directly connected to A7, A15, E23, A21



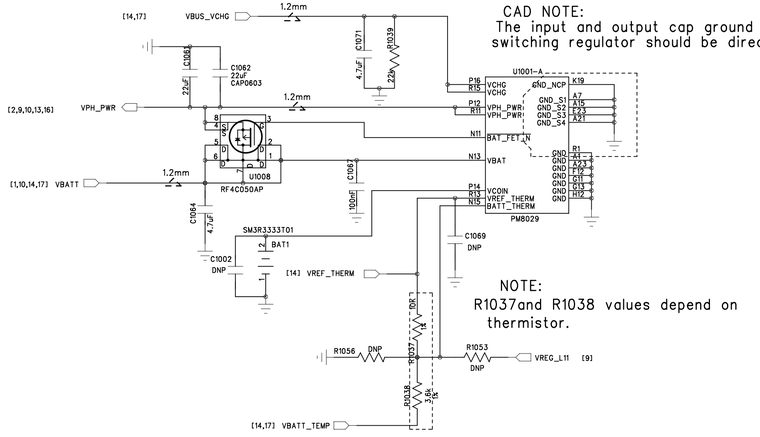








CAD NOTE:
The input and output cap ground of each switching regulator should be directly connected to these pins



NOTE:
R1037and R1038 values depend on thermistor.

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY:

TITLE:

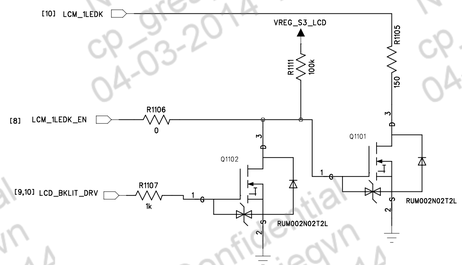
PMU PM8029

CODE:	SIZE:	DRAWING NO:	REV:

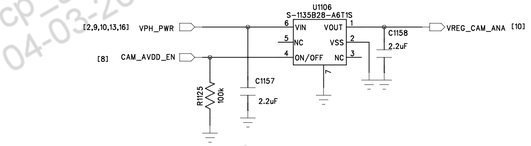
SCALE:

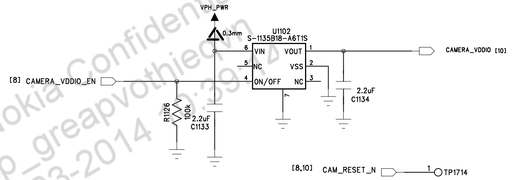
SHEET: 10 OF 16

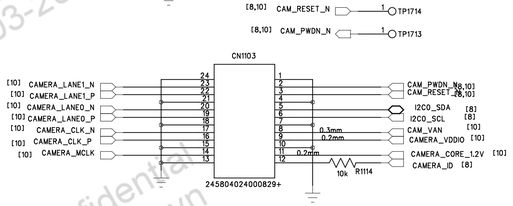
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

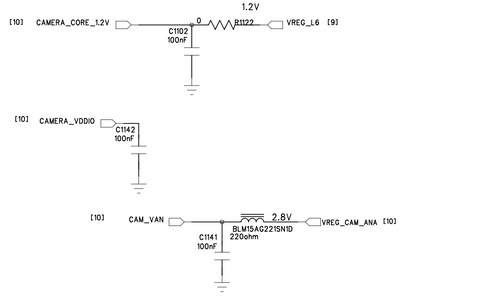


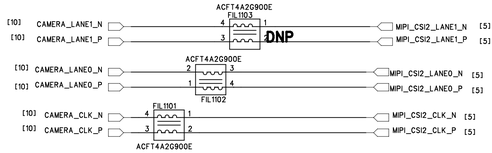
One LED enable

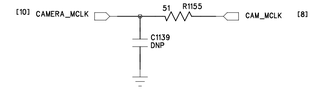








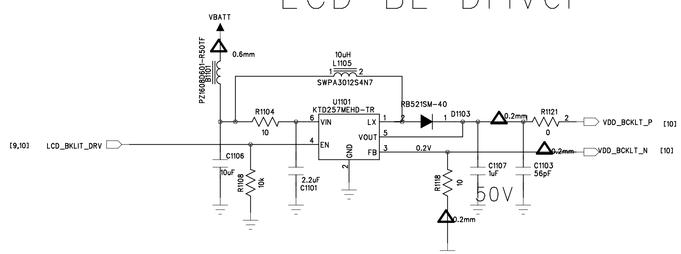




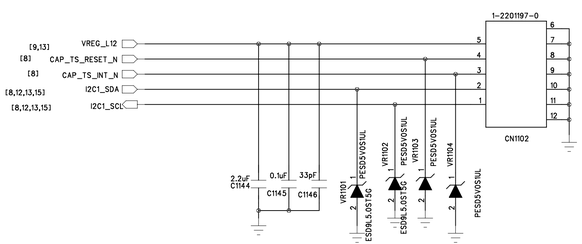
Model No:

I2C Addr:
write:; read:

LCD BL Driver



TP Connector



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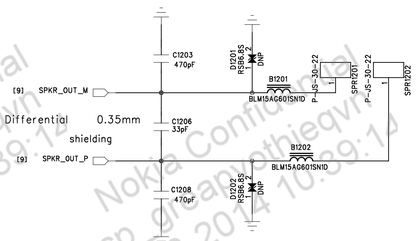
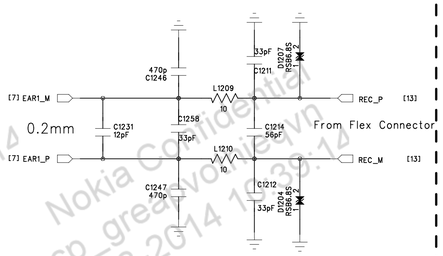
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: 11 OF 16

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

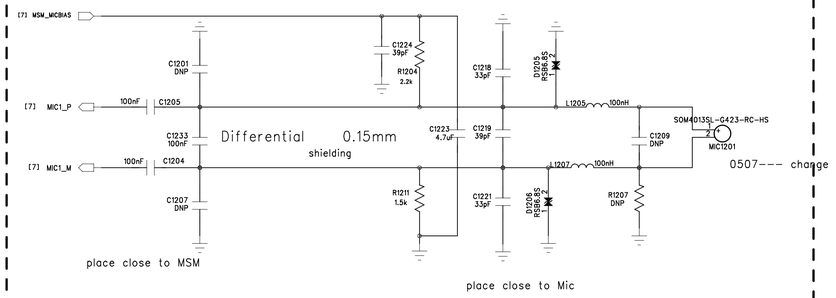
SPEAKER



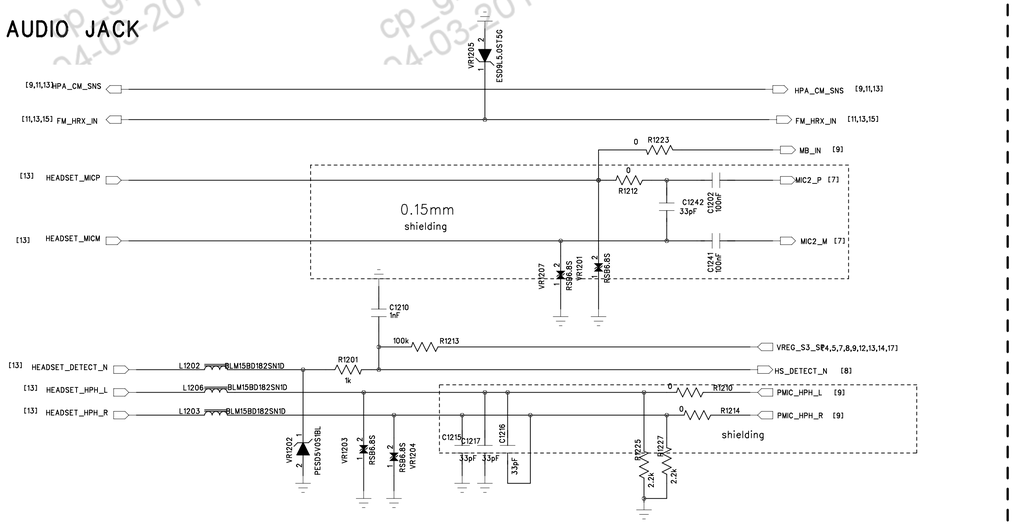
Receiver

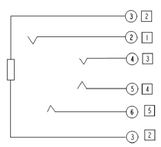


Microphone



AUDIO JACK





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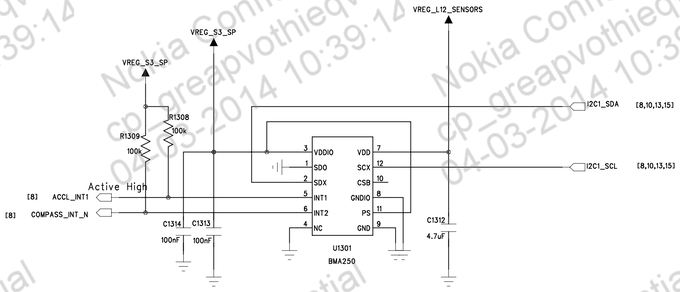
RELEASED:	DATED:	SCALE:	SHEET: 12 OF 16

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

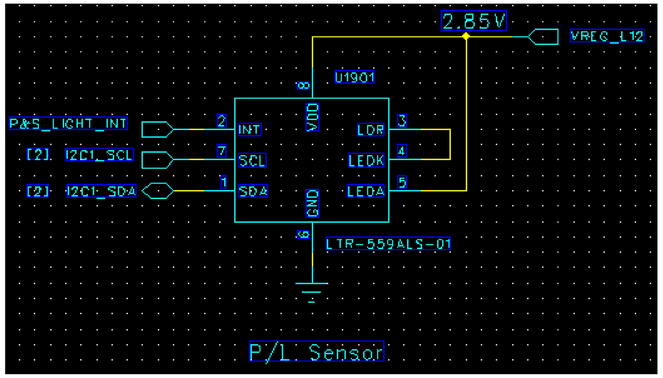
G sensor

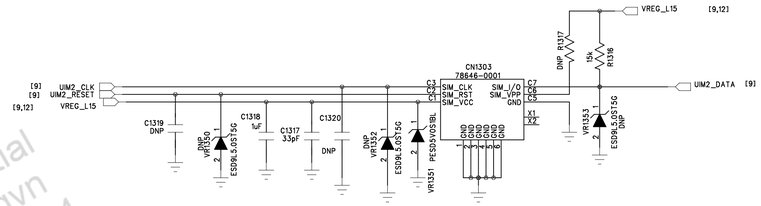


G Sensor
Slave address: 0x18H

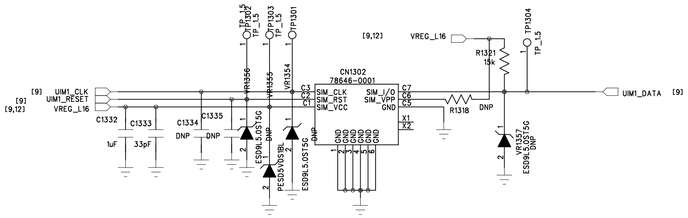
P/L sensor

P/L Sensor on Flex
The 7 bits slave address for this sensor is 0x23H





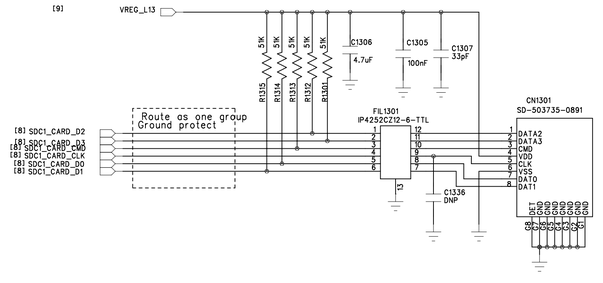
RUIM2_GSM



RUIM1_CDMA

PIN NO.	ASSIGNMENT
C1	Vcc (SUPPLY VOLTAGE)
C2	RST (RESET SIGNAL)
C3	CLK (CLOCK SIGNAL)
C4	RESERVED
C5	GND
C6	Vpp (VARIABLE SUPPLY VOLTAGE)
C7	I/O (DATA INPUT/OUTPUT)
C8	RESERVED
X1	NOT GND, FOR HOLD DOWN ONLY. (NOTE:X1 IS LINKED TO C1)
X2	NOT GND, FOR HOLD DOWN ONLY. (NOTE:X2 IS LINKED TO C3)

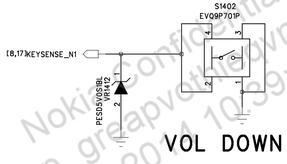
MICRO SD



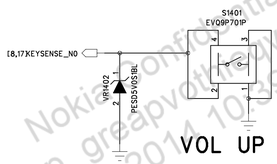
COMPANY:			
TITLE:	SENSOR SD RUIM		
DRAWN:	DATED:	CODE:	SIZE: DRAWING NO: REV:
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: 13 OF 16

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

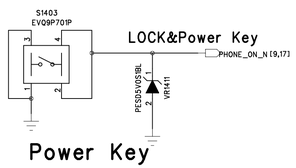
	Down to GND
GPIO36 KEYSENSE_N0	V+
GPIO37 KEYSENSE_N1	V−
	LOCK&Power Key



VOL DOWN

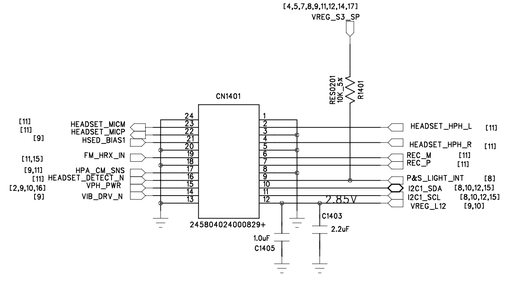


VOL UP



Power Key

Main board to Flex Connector



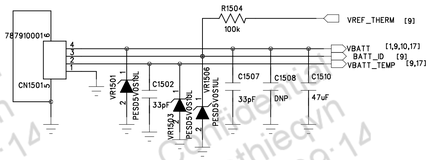
Need to check with flex

Flex part list:

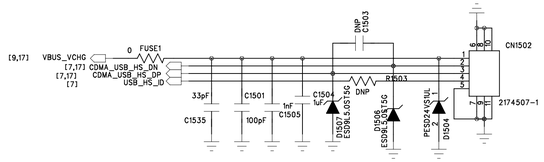
1. Receiver
2. Vibrator
3. Audio Jack
4. P/L Sensor

DRAWN:	DATED:	COMPANY:	
CHECKED:	DATED:	TITLE: KEYPAD and Flex connector	
QUALITY CONTROL:	DATED:	CODE: / SIZE: / DRAWING NO: / REV:	
RELEASED:	DATED:	SCALE:	SHEET: 14 OF 16

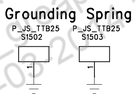
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

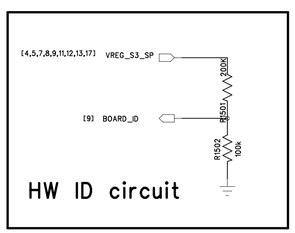


LESD9L5.0T5G



Micro_USB



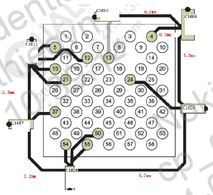


HW ID circuit

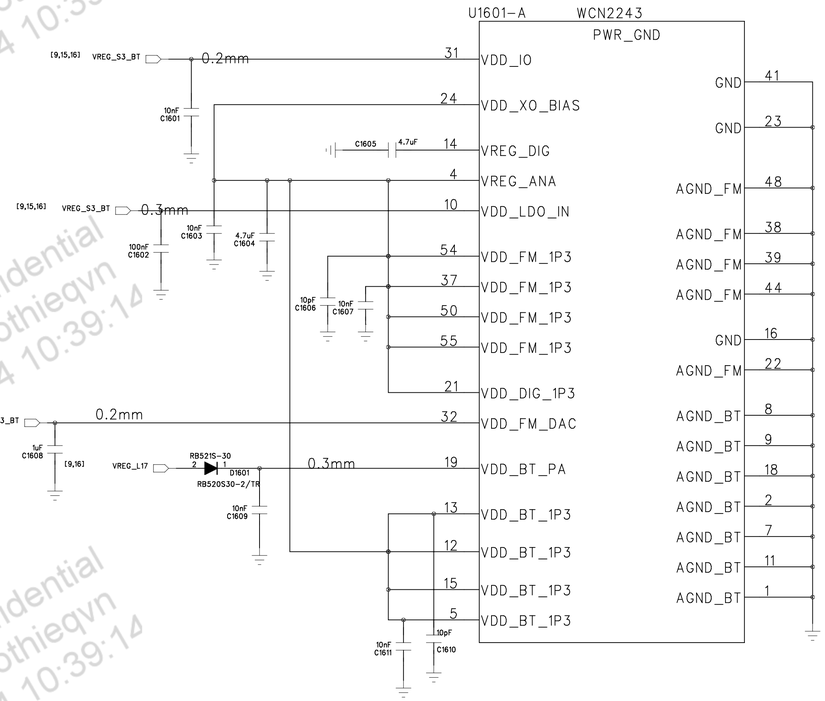
Build	MPP port	R1501 (Unit:Kohm)	R1502 (Unit:Kohm)	Refer voltage (Unit:V)	ADC voltage (Unit:V)	HW ID	GSM P A
B1	MPP8	200	510 Kohm	1.8V	1.3	0101	
		200	680 Kohm		1.4	0103	
		200	1 Mohm		1.5	0105	
S1.1	MPP8	200	300 Kohm	1.8V	1.1	0111	SKY77584
B2	MPP8	200	200 Kohm	1.8V	0.9	0201	SKY77584
		200	250 Kohm		1	0203	RF3237
B2.1	MPP8	200	400 Kohm	1.8V	1.2	0211	SKY77584
		200	250 Kohm		1	0203	RF3237
B3	MPP8	200	75 Kohm	1.8V	0.5	0301	
		200	100 Kohm		0.6	0303	
		200	127 Kohm		0.7	0305	
		200	160 Kohm		0.8	0307	
LV	MPP8	DNP	0	1.8V	0	0401	
		200	40 Kohm		0.3	0403	
		200	55 Kohm		0.4	0405	
MP	MPP8	DNP	0	1.8V	0	0501	
		200	40 Kohm		0.3	0503	
		200	55 Kohm		0.4	0505	

DRAWN:	DATED:	COMPANY:	
CHECKED:	DATED:	TITLE: USB BAT OVP	
QUALITY CONTROL:	DATED:	CODE:	SIZE: DRAWING NO: REV:
RELEASED:	DATED:	SCALE:	SHEET: 15 OF 16

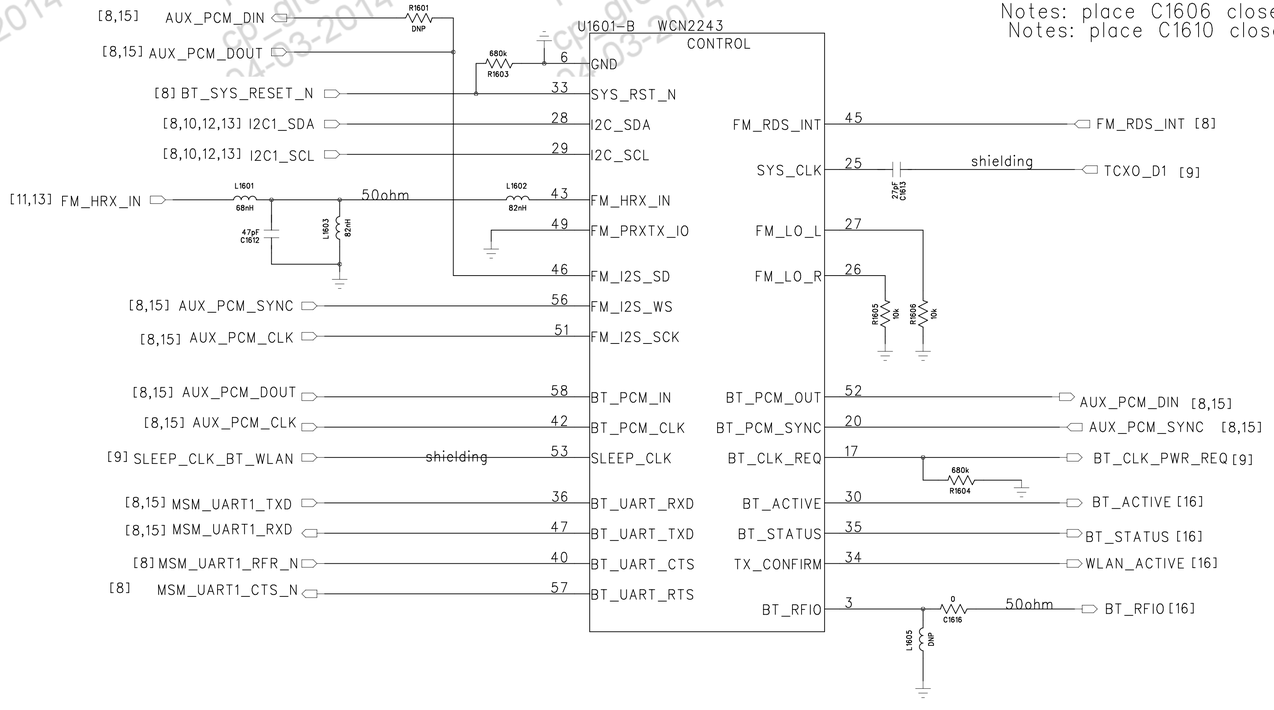
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



I2C ADDRESS: 0X0C



Notes: place C1606 close to Pin37 and C1607 close to Pin 54
Notes: place C1610 close to Pin13 and C1611 close to Pin 5



TP1704 1 MSM_UART1_RXD [8,15]
TP1705 1 MSM_UART1_TXD [8,15]

DRAWN:	DATED:
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:

COMPANY:

TITLE: **BT and FM**

CODE:	SIZE:	DRAWING NO:	REV:

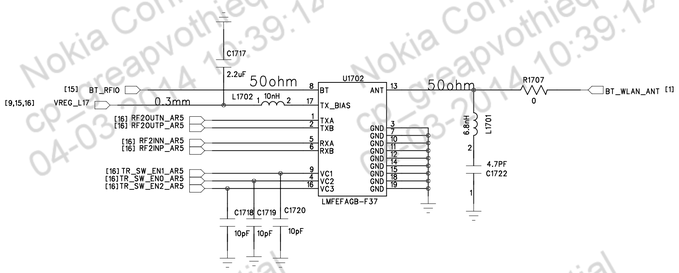
SCALE:

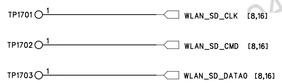
SHEET: 8 OF 12

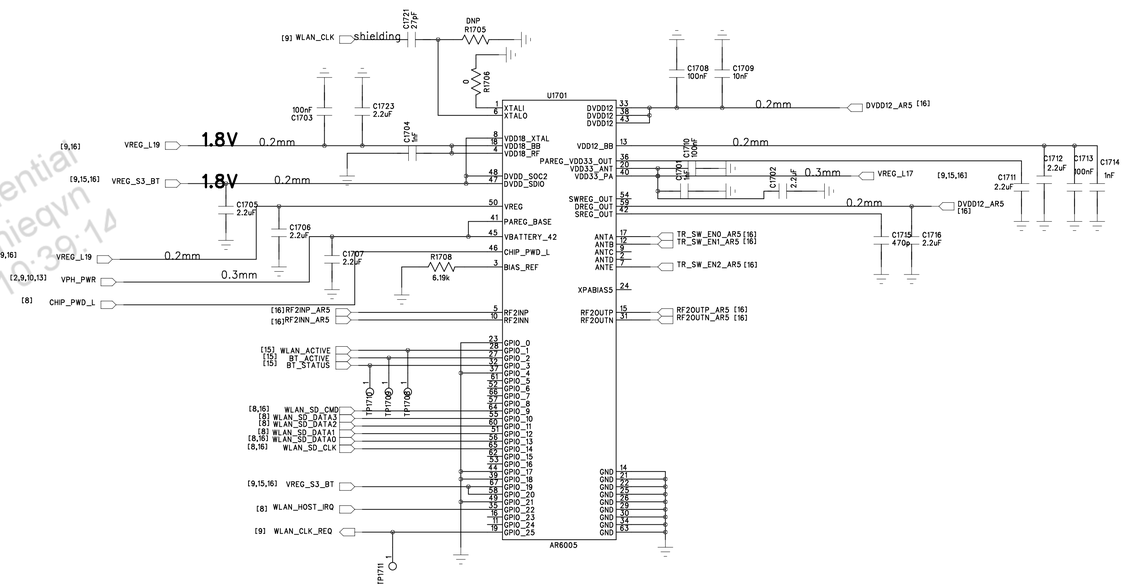
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

- For RF2INP and RF2INN layout follow these guidelines:
  a) Trace length must keep 75 mils (1.9mm) for each line from AR6005 to FEM.
  b) Trace to trace spacing must keep 10 mils (0.254mm).
- For RF2OUTP and RF2OUTN layout follow these guidelines:
  a) Trace length must be 80 mils (2.03mm) for each line from AR6005 to FEM.
  b) Trace to trace spacing must keep 10 mils (0.254mm).

these capacitors can be removed. It is highly suggested to keep on the board.







DRAWN:	DATED:	COMPANY:		
		TITLE: WIFI		
CHECKED:	DATED:	CODE:	SIZE:	DRAWING NO: / REV:
QUALITY CONTROL:	DATED:			
RELEASED:	DATED:	SCALE:	SHEET: 8 OF 12	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

[4,5,7,8,9,11,12,13,14,17] VREG_S3_SP — TP_1.0X1.8 TP6

[4] QFUSE_PWR — TP_1.0X1.8 TP5

Factory test point

[8] FORCE_DOWNLOAD — TP1509 TP_1.5

TP1510 TP_1.5

[9,13] PHONE_ON_N — TP1511 TP_1.5

[1,9,10,14] VBATT — VBAT TP_1.5

[9,14] VBATT_TEMP — TBAT TP_1.5

FID1 FIDUCIAL
FID2 FIDUCIAL
FID3 FIDUCIAL
FID4 FIDUCIAL

DRI1 DRILL_1.7_UP
DRI2 DRILL_1.9_UP
DRI3 DRILL_1.9_UP
DRI4 DRILL_2.0_UP

[9,14] VBUS_VCHG — TP1507 TP_1.5
[7,14] CDMA_USB_HS_DP — TP1503 TP_1.5
[7,14] CDMA_USB_HS_DN — TP1501 TP_1.5
TP3 TP_1.5

USB test point

[8,13] KEYSENSE_NO — TP1 TP_1.5

VOL UP

[8,13] KEYSENSE_N1 — TP2 TP_1.5

VOL Down

Direct to Switch

BRE1 BREAKAWAY_3_ND
BRE2 BREAKAWAY_3_ND
BRE3 BREAKAWAY_3_ND
BRE4 BREAKAWAY_3_ND
BRE5 BREAKAWAY_3_ND
BRE6 BREAKAWAY_3_ND
BRE7 BREAKAWAY_3_ND
BRE8 BREAKAWAY_3_ND
BRE9 BREAKAWAY_3_ND

JTAG Interface

Software debug

[5] JTAG_TDO — 1
[5] JTAG_TCK — 2
[5] JTAG_TDI — 3
[9] JTAG_PS_HOLD — 4
[5] JTAG_RTCK — 5
[5] JTAG_TMS — 6
[5] JTAG_TRST_N — 7
[7] JTAG_RESOUT_N — 8
[4,5,7,8,9,11,12,13,14,17] VREG_S3_SP — 9
10

CN1 FH19S-10S-0.7SH-N

Hot Bar

SCH1805 N_RF
SCH1806 N_GPS
SCH1804 N_RF_TRANSCEIVER
SCH1803 N_BT
SCH1802 N_PMU
SCH1801 N_CPU

Shielding

DRAWN:	DATED:	COMPANY:			
		TITLE: OTHER			
CHECKED:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
QUALITY CONTROL:	DATED:				
RELEASED:	DATED:	SCALE:		SHEET: OF	

Placements - Main board